WHAT IS CLAIMED IS:

1. A logic verification system utilizing the same FPGA module and the same configuration data in a couple of verification processes of logic emulation and logic simulation.

2. A logic verification system comprising:

a logic simulation accelerator including:

a device operating on a general purpose processor;

a device including a programmable logic device using FPGAs; and

a bridge circuit for transmitting and receiving data between said device operating on said general purpose processor and said device including the programmable logic device using said FPGAs,

wherein when the FPGA module used in the verification process in said logic emulator and the bridge circuit are wired in direct for all pins of said FPGA module and the logic simulation is accelerated, the cutting end of the verification logic is assigned to an external interface connector of the FPGA module, and the correspondence between each pin of the external interface connector of said FPGA module and logic signal is performed on said logic simulator on said general purpose processor.

3. The logic verification system according to claim 2, wherein the logic mounted on said FPGA module is

provided with a means for transmitting a direction control signal of two-way signal controlled therewith to the bridge circuit using an interface.

4. The logic verification system according to claim 2, wherein a means for automatically detecting a signal direction of two-way signal between said FPGA module and the device mounting the bridge circuit is provided, and the program data of the same FPGA group mounting the verification object logic is used in a couple of verification processes of the acceleration of logic simulation and logic emulation.

5. The logic verification system according to claim 4, wherein said means for automatically detecting the signal direction of two-way signal between said devices is capable of setting a drivability level of output circuits of both devices and giving the priority in determination of signal direction to the device having higher drivability.

6. The logic verification system according to claim 4, comprising: a means for automatically detecting signal direction of two-way signal between said FPGA module and the device mounting the bridge circuit; and a means for inputting signal direction of two-way signal to the logic simulator on the general purpose processor,

wherein the signal direction of logic simulator and disagreement of signal direction in the FPGA module is detected by comparing said two signal directions.

7. The logic verification system according to claim 6, wherein said means for automatically detecting signal direction of two-way signal between said devices is capable of setting a drivability level of output circuits of both devices and giving the priority in determination of signal direction ot the device having higher drivability.